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Jessica Haglund and John F. Conley, Jr.[a)]

AFFILIATIONS

School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, Oregon 97331, USA

[a)]**Author to whom correspondence should be addressed:** jconley@eecs.oregonstate.edu

ABSTRACT

Metal/insulator interfaces impact the performance of electron devices through a variety of process dependent extrinsic effects. Bilayer-metal electrodes employing a reactive interfacial metal are often used to promote the adhesion of an overlying inert cap metal to an oxide. Bilayer-metal stacks have been proposed to decouple the influence of some extrinsic effects, such as interfacial defects from others such as strain and metal grain size, to assist in the optimization of silicon quantum bits. In this work, we used internal photoemission spectroscopy to directly measure the influence of the interfacial Ti thickness on the electron energy barrier at the Pt/Ti/Al_2O_3 bilayer-metal/insulator interface of Pt/Ti/Al_2O_3/TiN devices. We found that a 0.5 to 1.0 nm thick layer of Ti was sufficient to completely dominate the electron energy barrier. Insertion of a Ti layer also resulted in band tailing, likely due to oxygen scavenging, but had no impact on the bottom Al_2O_3/TiN electrode barrier.

I. INTRODUCTION

Owing to the long coherence times for electron spins and the highly advanced state of silicon microelectronics, silicon remains one of the most promising materials for quantum computing.[1,2] One of the most practical approaches to quantum bit (qubit) formation in Si is electrostatic gating using a surface metal over a thin dielectric.[3,4] The threshold voltage, V_T, of an electrostatically defined qubit, as with metal–oxide–semiconductor field-effect transistors (MOSFETs), is controlled in part by the interface between the metal and insulator. Ideally, the electron energy barrier, φ_{Bn}, at a metal/insulator interface should be determined solely by the difference between the metal vacuum work function, $\Phi_{M,vac}$, and the insulator electron affinity, χ_i, where $\varphi_{Bn} = \Phi_{M,vac} - \chi_i$. However, this is rarely the case. Instead, φ_{Bn}'s are often influenced by induced virtual gap states as well as *extrinsic* effects such as interfacial and near-interfacial trapped charge arising from point defects, dipoles (due to interfacial chemical reactions), scavenging of oxygen from the insulator, Fermi level pinning, metal grain size, and thermal mismatch, all of which are affected by processing. A metal on an insulator, thus, often behaves as if it has an effective work function, $\Phi_{M,eff}$, such that $\varphi_{Bn} = \Phi_{M,eff} - \chi_i$.[5] Precise knowledge of φ_{bn}'s is critical for understanding, predicting, and optimizing the performance of devices such as metal/insulator/metal (MIM) capacitors and diodes, ferroelectric tunnel junctions (FTJs), MOSFETs, MOS capacitors, and electrostatically defined qubits. Because φ_{bn}'s can depend intimately on processing history, they are not straightforward to theoretically predict and it is necessary to directly measure φ_{Bn} for the *specific* metal/insulator combination in use.[6] Although they can be estimated with electrical measurements and x-ray photoelectron spectroscopy, the only technique capable of *direct in situ* measurement of φ_{Bn}'s in operating devices is internal photoemission (IPE) spectroscopy, an optoelectronic technique involving measurements of photocurrent in a biased device while under ultraviolet illumination.[7–14]

Optimizing metal/insulator contacts typically involves trade-offs between the various mentioned nonidealities and can be difficult to achieve using a single metal gate. Metal-bilayers, consisting of a thick capping metal over a thin interfacial metal, have been proposed as a way to optimize qubit performance by separating the cap metal from the interface in order to decouple work function, strain, grains, and interfacial defects.[15] The bilayer-metal technique is widely used to promote adhesion of a large work function inert metal to an oxide by using a thin "wetting" metal at the interface. Electrical studies have indicated that the presence of a very thin metal at the metal-bilayer/insulator interface can have a large impact on $\Phi_{M,\text{eff}}$.[16–19] In those studies, $\Phi_{M,\text{eff}}$ was indirectly estimated from the flatband voltage, V_{FB}, of capacitance vs voltage (CV) measurements and required a series of MOS devices with different oxide thickness as well as assumptions about and modeling of oxide and interface charge.[20] Although IPE measurements have been reported on bilayer stacks with overlying high diffusivity Cu based metals,[21] TiN layer based bilayer stacks,[22,23] and even amorphous metals (where there are no grains),[24,25] the influence of the interfacial metal thickness on φ_{Bn} has not been systematically investigated using IPE, particularly for metals such as Pt, which are of relevance to electrostatically defined qubits.[15]

In this work, we report direct IPE measurements of φ_{Bn} at both the top and bottom interfaces of a series of Pt/Ti bilayer-metal/Al_2O_3/TiN MIM devices as a function of Ti interfacial metal thickness for two different thicknesses of atomic layer deposited (ALD) Al_2O_3.

II. EXPERIMENTAL

Device fabrication began with deposition of a 100 nm thick TiN blanket bottom electrode via reactive ion sputtering of a Ti target in N_2. Al_2O_3 was then deposited on the TiN via ALD in a Picosun R-200 reactor at 250 °C. Trimethylaluminum [$Al(CH_3)_3$, TMA] and H_2O were used as precursors. One ALD cycle consisted of an alternating pulse sequence of TMA (0.1 s)/N_2 purge (10 s)/H_2O (0.1 s)/N_2 purge (10 s). Samples with Al_2O_3 thicknesses of either 8.7 or 17.8 nm were deposited with 100 and 200 cycles ALD cycles, respectively. Al_2O_3 film thickness and refractive index were measured across Si witness coupons using a Film Sense FS-1 multiwavelength mapping ellipsometer using a Cauchy model on Si with a native oxide. The native oxide thickness was measured prior to deposition.

Following Al_2O_3 deposition, vacuum was broken and samples were transferred to a load-locked electron beam deposition tool where semitransparent bilayer Pt/Ti top electrodes were sequentially deposited by electron beam deposition through a shadow mask at room temperature, resulting in 50, 125, 250, and 500 μm diameter circular devices. Ti adhesion layer thicknesses, d_{Ti}, of either 0, 0.5, 1, 2.5, 5, or 10 nm were followed by 10 nm of Pt. Prior to Ti and Pt deposition, Ti or Pt, respectively, was evaporated for approximately 30 s before opening the sample shutter. Cross-sectional TEM images, taken across the center of Pt/Ti/Al_2O_3/TiN MIM devices with Ti thicknesses of (a) ~0.5 and (b) 10 nm, respectively, both with ~8.7 nm of Al_2O_3, are shown in Fig. 1. The slight difference in the Pt thickness between Figs. 1(a) and 1(b) was due to a slight deposition non-uniformity—areas of a sample further away from the center of the chamber were somewhat thinner. Due to this systematic thickness variation, the very thin ~0.5 nm Ti layer in Fig. 1(a) may not have been continuous across all the devices on all coupons. All devices were measured as-deposited, with no postmetallization annealing.

Capacitance vs voltage (CV) measurements on the completed Pt/Ti/Al_2O_3/TiN/Si MIM devices were conducted in a probe

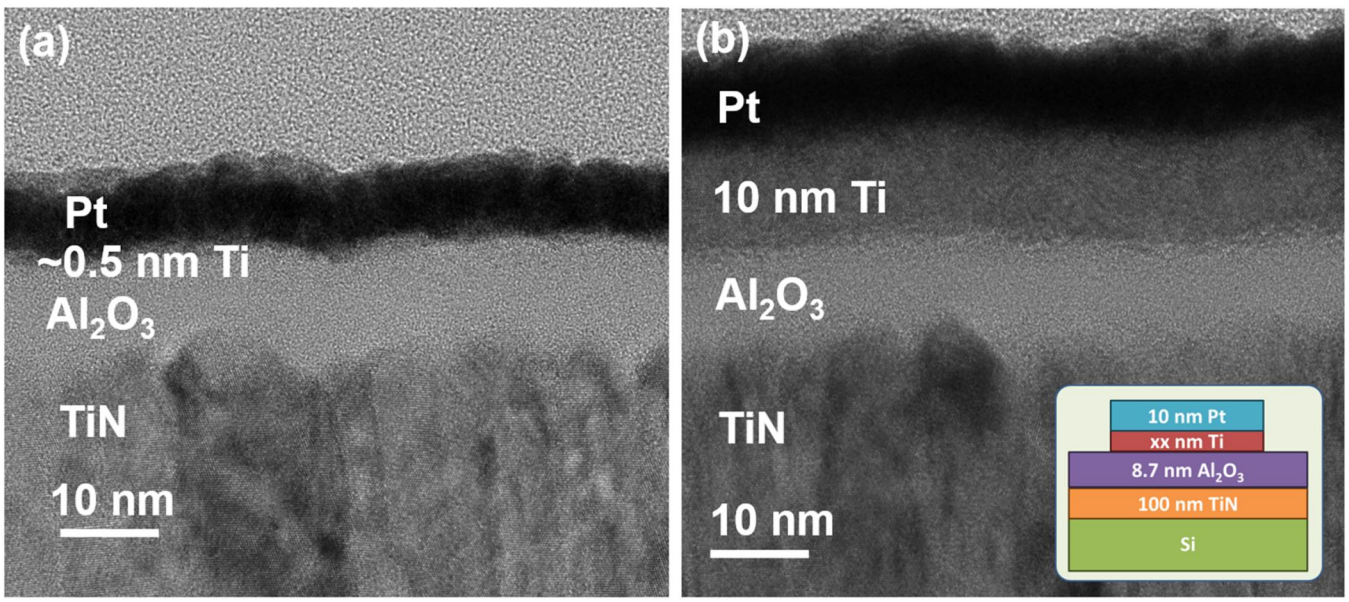

FIG. 1. Cross-sectional TEM images for Pt/Ti/Al_2O_3/TiN devices with 100 cycles of Al_2O_3 and (a) d_{Ti} = 0.5 nm and (b) d_{Ti} = 10 nm.

station in the dark using an Agilent 4284 A. IPE measurements were performed using a lab built system described previously.[14,25] Summarily, light from a 150 W Xe arc lamp was passed through a Princeton Instrument SP2150i monochromator and then through bandpass filters before being focused with a mirror onto the top electrode of the MIM devices. To measure IPE from the top (bottom) electrode, voltage was stepped from 0 to −2 V (+2 V) in −0.1 V (+0.1 V) increments using a Yokogawa GS200 DC voltage source. Fresh devices were used for top and bottom barrier measurements. For each applied bias, the average dark current, I_{dark}, was first determined by taking a 30 s average of the current in the dark. Then, the photon energy, E_{ph}, was swept from 1.7 to 5.5 eV in 0.1 eV steps and the average current, I_{IPE}, was measured at each E_{ph}. Current was measured using a Keithley 617 electrometer. The IPE quantum yield, Y, at each photon energy was taken as $Y = \frac{(I_{IPE} - I_{dark}) * E_{ph}}{P_{lamp}(E_{ph})}$, where $P_{lamp}(E_{ph})$ is the power of the lamp at each photon energy. A plot of $Y^{1/2}$ (for emission from a metal)[7,26] vs E_{ph} was used to determine the onset threshold, φ_{thresh}, of IPE at each field. The electric field across the Al_2O_3 ($\xi_{Al_2O_3}$) was determined by subtracting built-in voltage across Al_2O_3 due to the electrode effective work function difference, V_{bi}, from each applied voltage and then dividing by the Al_2O_3 thickness. V_{bi} was determined as the applied voltage at which I_{dark} switches from negative to positive. Finally, φ_{thresh} values were plotted vs $\xi_{Al_2O_3}^{1/2}$ and a linear fit was used to extrapolate zero field ($\xi_{Al_2O_3} = 0$) electron barrier heights, φ_{Bn}, which in this work represents the energy difference between the Fermi level of the respective metal gate and the conduction band edge of Al_2O_3. IPE φ_{Bn} estimation error is estimated at roughly ±0.1 eV for comparing different devices and less than ±0.03 eV for repeated measurements on the same device.

III. RESULTS

Shown in Fig. 2 are representative normalized IPE yield curves for Pt/Ti/Al_2O_3/TiN devices with various d_{Ti}. Negative

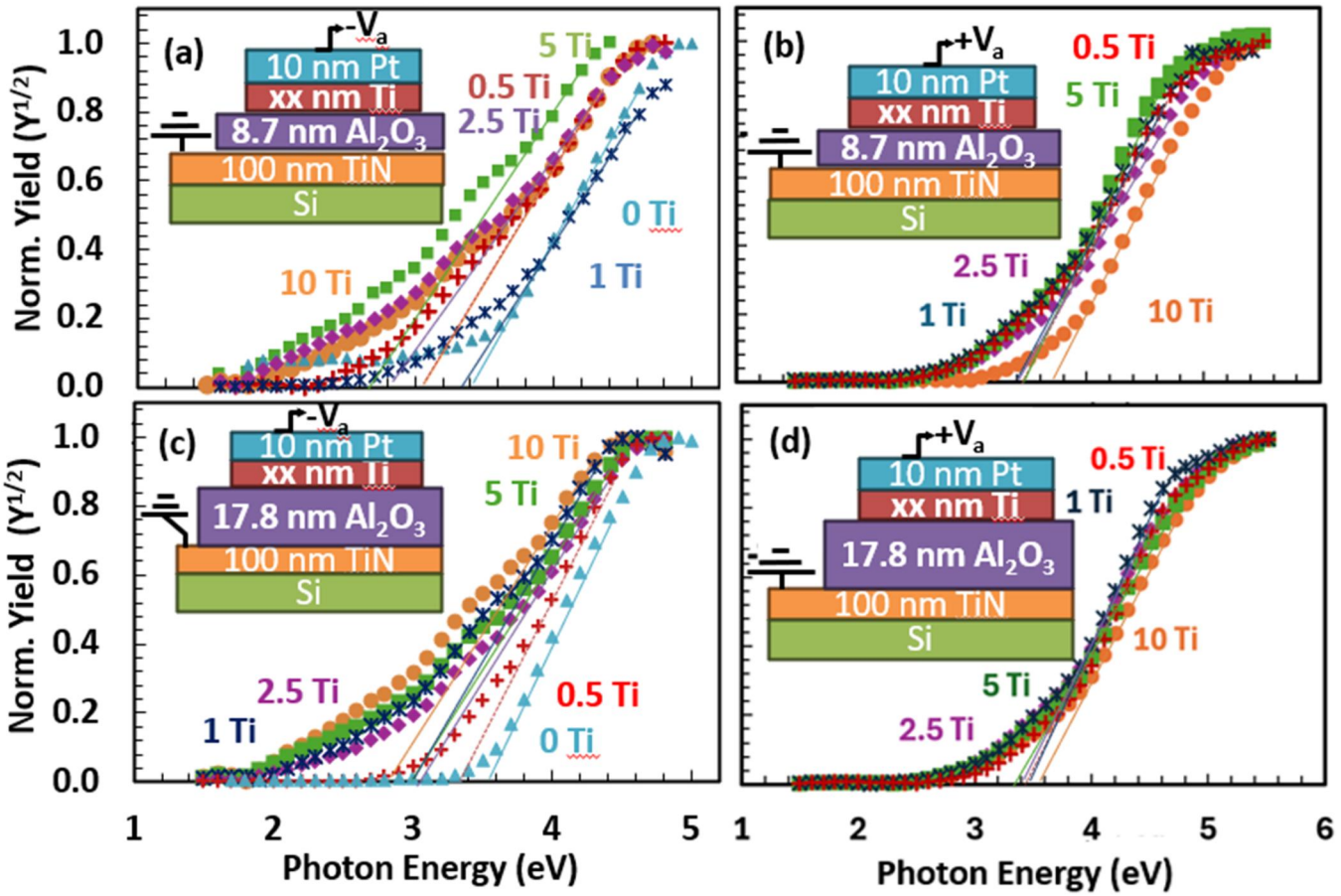

FIG. 2. Representative normalized IPE square root yield plots for Pt/Ti/Al_2O_3/TiN devices with various d_{Ti} (indicated) and either (a) 8.7 nm or (c) 17.8 nm of Al_2O_3 under negative polarity (−1.0 MV/cm) and (b) 8.7 nm or (d) 17.8 nm of Al_2O_3 under positive polarity (+1 MV/cm). The symbols are as follows: 0 nm Ti (blue triangle) 0.5 nm Ti (red cross), 1 nm Ti (blue asterisk), 2.5 nm Ti (purple diamond), 5 nm Ti (green square), 10 nm (orange circle). Linear fit lines are shown to indicate the data points used to determine φ_{thresh} (the *x*-axis intercept).

polarity (−1 MV/cm) curves, characterizing electron emission across the top interface, are shown for devices with either 8.7 [Fig. 2(a)] or 17.8 nm [Fig. 2(c)] of Al_2O_3. In both cases, devices without a Ti wetting layer ($d_{Ti} = 0$ nm) exhibited a sharp IPE emission threshold. The inclusion of a thin ~0.5 nm Ti layer resulted in a reduction of φ_{thresh} and the appearance of a low energy tail. For the 17.8 nm Al_2O_3 devices, 1 nm of Ti resulted in a further reduction in φ_{thresh}, increased tailing, and the appearance of a slight "hump" in the range of 3–3.8 eV. Despite these changes, there was no change in leakage current with all devices showing $I_{dark} < 1$ pA. The apparent out-of-step progression of the ~0.5 and ~1.0 nm Ti yield curves for the 8.7 nm Al_2O_3 devices in Fig. 2(a) was likely due to slight thickness variations in the thin Ti film across the wafer. For $d_{Ti} \geq 2$ nm, little further change in φ_{thresh} was produced. However, there was a subtle evolution in the shape of the yield curves, seen more distinctly in the 17.8 nm devices. As discussed below, the tailing/hump region is likely due to defects created at or near the Ti/Al_2O_3 interface. The slope increase above the hump represents emission from the metal into the Al_2O_3 conduction band and was the region from which φ_{thresh} values were extrapolated.

Also shown in Fig. 2 are representative positive polarity (+1 MV/cm) normalized IPE yield curves for Pt/Ti/Al_2O_3/TiN devices with various d_{Ti} and either 8.7 [Fig. 2(b)] or 17.8 nm [Fig. 2(d)] of Al_2O_3. In contrast to emission from the top electrode and consistent with expectations, the Ti layer at the top interface had no impact on the bottom electrode φ_{thresh} values or yield curves.

Schottky plots of field dependent φ_{thresh} values vs $\xi_{Al_2O_3}^{1/2}$ for all devices are shown in Fig. 3. φ_{Bn} were determined by extrapolating each plot to $\xi_{Al_2O_3}^{1/2} = 0$, thus accounting for any field induced barrier lowering.

Plots of φ_{Bn} vs d_{Ti} for top and bottom interfaces is shown in Figs. 4(a) and Fig. 4(b), respectively, and φ_{Bn} values are summarized in Table I. Consider first the electron emission at the top (Pt/Ti/Al_2O_3) interface. In the absence of Ti ($d_{Ti} = 0$ nm), $\varphi_{Bn,Pt/Al_2O_3}$ was in the range of 3.5–3.6 eV. The only other reported IPE φ_{Bn} values for a direct Pt/Al_2O_3 interface (with sputtered Pt and 19 nm thick ALD Al_2O_3) were 3.3 or 2.9 eV following 400 °C anneals in either vacuum or H_2, respectively.[26] The barrier here for e-beam Pt with 20 nm Al_2O_3 was 3.6 eV, larger than this previous report but near the low end of the 3.7–4.6 eV range calculated

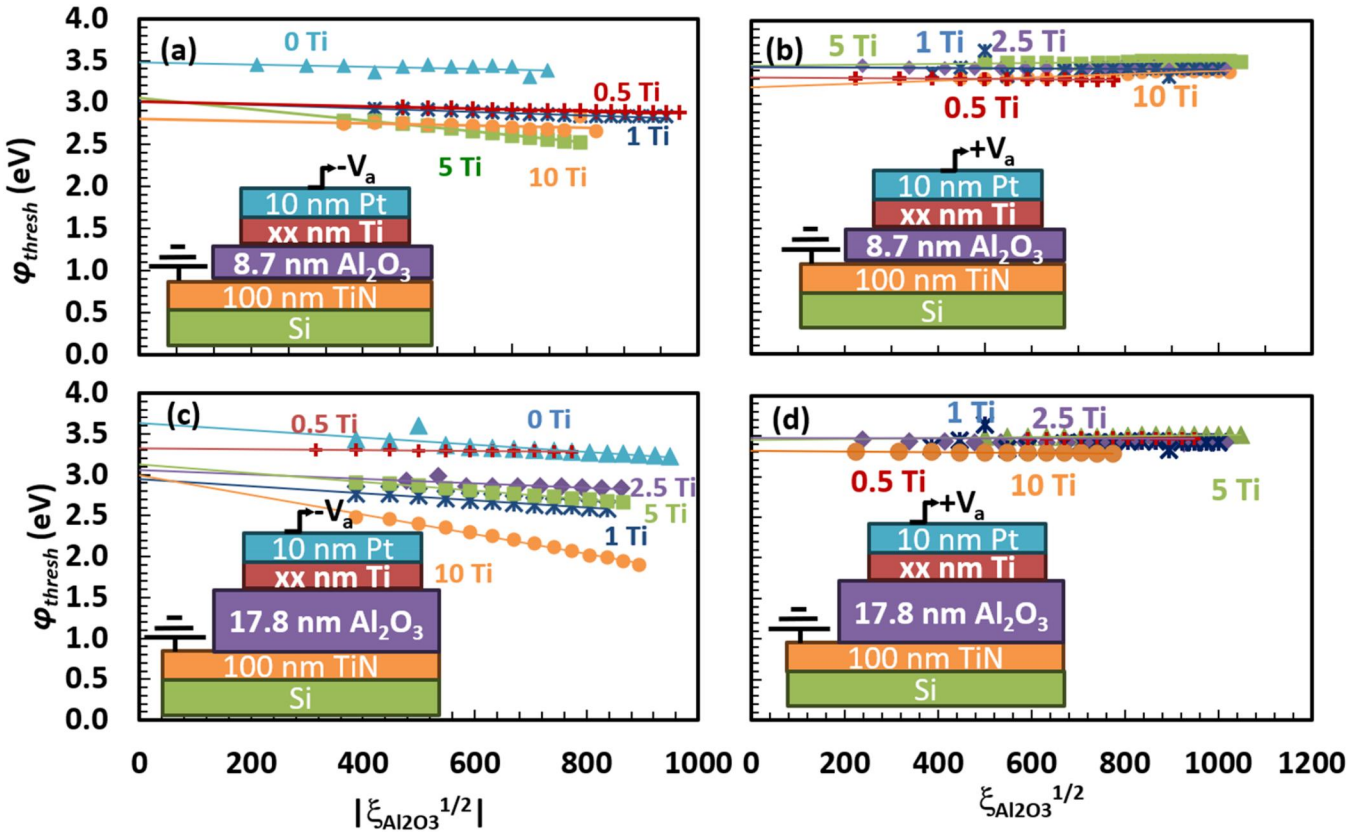

FIG. 3. Schottky plots of φ_{thresh} vs $|\xi_{Al_2O_3}^{1/2}|$ for Pt/Ti/Al_2O_3/TiN MIM devices with various d_{Ti} (indicated) and either (a) 8.7 nm or (c) 17.8 nm of Al_2O_3 under negative polarity and (b) 8.7 nm or (d) 17.8 nm of Al_2O_3 under positive polarity. The symbols are as follows: 0 nm Ti (blue triangle) 0.5 nm Ti (red cross), 1 nm Ti (blue asterisk), 2.5 nm Ti (purple diamond), 5 nm Ti (green square), 10 nm (orange circle).

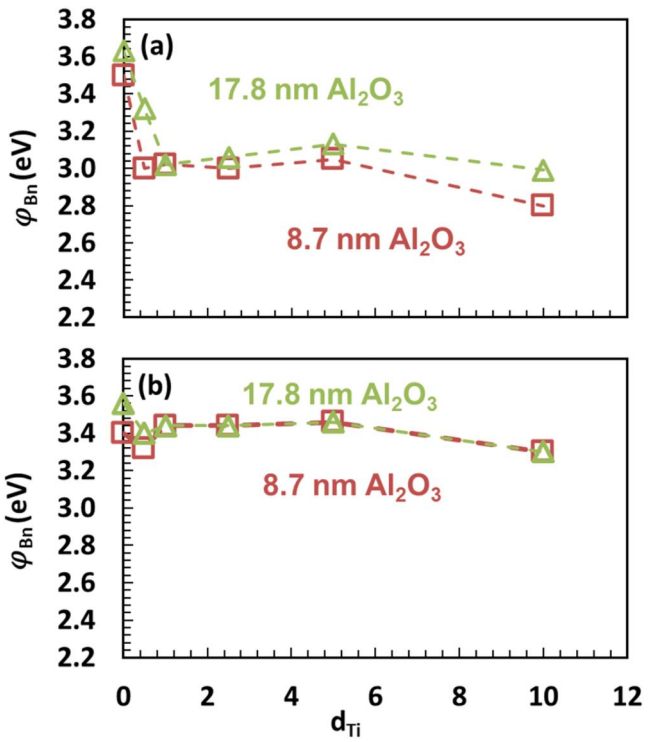

FIG. 4. φ_{Bn} vs d_{Ti} plots for Pt/Ti/Al_2O_3/TiN MIM devices with either 8.7 or 18.7 nm of Al_2O_3 (symbol size encompasses error bars) for both the (a) Pt/Ti/Al_2O_3 top and (b) bottom Al_2O_3/TiN bottom electron barriers. In these plots, 8.7 nm Al_2O_3 is represented with red squares and 17.8 nm Al_2O_3 is represented by green triangles.

from Schottky–Mott theory, the difference between $\Phi_{Pt,vac}$ (5.6 eV) and $\chi_{Al_2O_3}$($\chi_{Al_2O_3}$ = 1.0–1.9 eV).[27–29] The different barrier heights observed among the Pt/Al_2O_3 interfaces in the previous and present report may be attributed to the different deposition methods, processing, or a process induced interfacial dipole, as postulated in Ref. 26.

The addition of a ~0.5–1.0 nm Ti wetting layer resulted in an approximately 0.5 eV reduction of $\varphi_{Bn,Pt/Ti/Al_2O_3}$ to 3.0 eV. For the 0.5 nm Ti sample, the higher barrier measured for the 17.8 vs 8.7 nm Al_2O_3 device (3.3 vs 3.0 eV, respectively), combined with the TEM result in Fig. 1, points to some mixing of Pt and Ti at the interface due to the very thin and thus potentially incomplete layer of Ti. A further increase in d_{Ti} produced little change in $\varphi_{Bn,Pt/Ti/Al_2O_3}$. Although φ_{thresh} values at a single field have been previously reported, there are no direct IPE reports of φ_{Bn} for the Ti/Al_2O_3 interface to compare.[23] However, our $\varphi_{Bn,Pt/Ti/Al_2O_3}$ value is the middle of the 2.4–3.3 eV range calculated from the difference between $\Phi_{Ti,vac}$ (=4.3 eV) and $\chi_{Al_2O_3}$.

For the bottom Al_2O_3/TiN interface, the Ti layer had little impact. $\varphi_{bn,TiN/Al_2O_3}$ remained at 3.4 eV ± 0.1 eV (within experimental error), independent of d_{Ti}. This was an indication that there is no remote scavenging of oxygen from the opposing interface. IPE reports for the TiN/Al_2O_3 interface range from 3.3 to 3.8 eV for *sputtered* TiN, roughly consistent with this result.[23,24,29] As the work function of TiN is process dependent, φ_{bn} will also be process dependent.

$\varphi_{Bn,Pt/Ti/Al_2O_3}$ for the 17.8 nm Al_2O_3 devices averaged a little more than 0.1 eV (ranging from 0 to 0.3 eV) greater than the barrier for the 8.7 nm Al_2O_3 devices. The difference is consistent with works that have shown that the electronic and optical properties of very thin ALD Al_2O_3 are a function of thickness, with layers thinner than ~10–15 nm exhibiting a lower dielectric constant, refractive index, and density.[30–32]

The fact that only ~1 nm of a Ti interfacial layer was sufficient to completely dominate $\varphi_{Bn,Pt/Ti/Al_2O_3}$ is consistent with *ab initio* calculations of metal stacks on SiO_2, which predicted that only one to three monolayers of interfacial metal should be sufficient to transition $\Phi_{M,eff}$ from that of the cap metal to the interfacial metal.[17] An abrupt transition is also consistent with several electrical studies. Based on V_{FB} measurements of Al/TaN/SiO_2/Si structures, Gao *et al.* showed that less than 6 nm of interfacial TaN was sufficient to transition $\Phi_{M,eff}$ from the Al cap to the TaN interfacial metal when unannealed, extending to 10 nm following a 400 °C postmetallization anneal.[16,33] Lu *et al.* also estimated $\Phi_{M,eff}$ from plots of V_{FB} vs effective oxide thickness (EOT). For Ti/W/SiO_2, they showed that <2.5 nm of interfacial W was sufficient to transition $\Phi_{M,eff}$ from the cap metal to interface metal when unannealed, extending to ~10 nm when annealed at 400 °C. For Ti/Pt/HfO_2 and Pt/Ti/HfO_2 as well as for Ti/Pt, Al/Ni, Ti/W, and Ta/TaN with SiO_2, they saw an approximately 6 nm transition to $\Phi_{M,eff}$ of the interfacial metal following 300 °C annealing.[19] They later reported a less than 2 nm transition for as-deposited W/Ti/SiO_2 and Ti/W/SiO_2 and demonstrated that $\Phi_{M,eff}$ tuning in bilayer-metal stacks was due to the diffusion of the cap metal to the interface region.[18] Similar results and conclusions were reported by Wu *et al.* on unannealed metal/TaN/Ge. They found that 5 nm of interfacial TaN was sufficient to completely dominate the Schottky barrier height (extracted from I–V modeling) of junctions with either Al, Ni, or Fe as the capping metal.[34]

Previous reports have shown that IPE spectral thresholds (φ_{thresh}) at a single fixed applied field for either Cu/(Hf, Ta, or Ti) or TiN_x/Ti bilayer electrodes with Al_2O_3 or SiO_2 were influenced by the thickness of the metal layer at the interface. However, these results did not report φ_{Bn} and were affected by either the high diffusivity of Cu and the relative diffusion barrier properties of the

TABLE I. Summary of $\varphi_{Bn,Pt/Ti/Al_2O_3}$ and $\varphi_{Bn,TiN/Al_2O_3}$ for various d_{Ti}.

	$\varphi_{Bn,Pt/Ti/Al_2O_3}$ (eV)		$\varphi_{Bn,Pt/TiN/Al_2O_3}$ (eV)	
d_{Ti} (nm)	8.7 nm Al_2O_3	18.7 nm Al_2O_3	8.7 nm Al_2O_3	18.7 nm Al_2O_3
0	3.50(3)	3.63(3)	3.40(3)	3.56(3)
~0.5	3.00(3)	3.32(3)	3.32(3)	3.36(3)
1	3.02(3)	3.02(3)	3.44(3)	3.43(3)
2	3.00(3)	3.06(3)	3.44(3)	3.44(3)
5	3.05(3)	3.13(3)	3.46(3)	3.47(3)
10	2.80(3)	2.99(3)	3.30(3)	3.32(3)

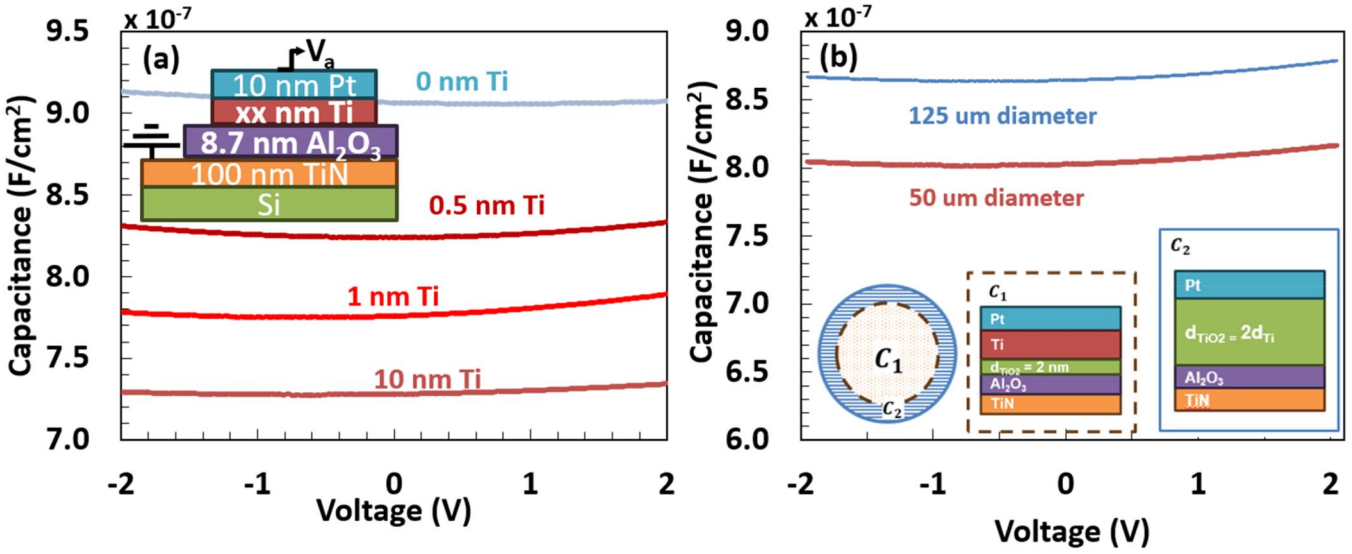

FIG. 5. Capacitance density vs voltage sweeps for Pt/Ti/Al_2O_3/TiN/Si devices with 8.7 nm Al_2O_3. (a) 5.2×10^{-4} cm^2 (~125 μm diameter) devices with various d_{Ti} and (b) 5.2×10^{-4} cm^2 and 1.4×10^{-4} cm^2 (~50 μm diameter) devices with $d_{Ti} = 10$ nm. The inset in (b) illustrates the two structures used for modeling the total capacitance. C_1 shows the inner circular capacitor of area A_{circ}, and C_2 shows the outer ring capacitor of area A_{ring}.

interfacial metal or nitridation of the interfacial Ti layer, respectively.[21,23] The present work is the first to directly and systematically show the impact of the interfacial metal thickness on IPE determined φ_{bn}.

Turning attention back to the early low energy tail and "hump" in the yield curves in Figs. 2(a) and 2(b) for devices with Ti layers, these features appear with the addition of 0.5 nm of Ti and increase only slightly with Ti thickness greater than 1 nm. They are present only for top electrode emission and are absent for bottom electrode emission and are, thus, likely the result of an interaction between Ti and Al_2O_3. Although the enthalpy of oxide formation of Al_2O_3 is more negative than that of TiO_2, the Gibbs free energy of oxide formation at room temperature favors TiO_2. The Ti layer will, thus, scavenge some oxygen from the top of Al_2O_3, forming TiO_x and a reduced AlO_x layer with an increased density of oxygen vacancies (V_O).[35,36] Indeed, Ti layers have been employed to engineer V_O density in Al_2O_3 resistive random access memory (RRAM) devices.[37] Reflective electron energy loss spectroscopy (REELS) shows that V_O can introduce levels throughout the gap of Al_2O_3, centered at about 1.4 eV below the conduction band.[38] DFT calculations and Frenkel–Poole emission results also indicate V_O levels at 1.1 and 1.4 eV below the conduction band, respectively.[39,40] It has also been shown that V_O can cause band tailing in Al_2O_3.[23] The V_O levels can serve as steppingstones into the Al_2O_3 conduction band, effectively stretching out the barrier and resulting in the observed yield tailing seen in Fig. 2.

Although the Ti oxidation process is favorable and fast, the diffusion barrier properties of the TiO_x ultimately self-limit its thickness to <6 nm at room temperature (and likely even thinner within the 6 month time frame of these experiments).[41,42] The limited oxidation means that thickness of TiO_x formed on Ti layers more than a few nm thick is likely independent of d_{Ti} and thus consistent with the observed lack of a strong d_{Ti} dependence of the tail and hump features.

Although the TEM images and accompanying EDS results (not shown) had insufficient resolution to provide evidence of oxidation, we can infer the presence of a TiO_x interfacial layer from CV measurements. Shown in Fig. 5(a) are CV curves for the Pt/Ti/Al_2O_3/TiN/Si devices from Figs. 2(a) and 2(b). Despite the fixed Al_2O_3 thickness, capacitance density decreased with increasing d_{Ti}. Reduced capacitance density is consistent with TiO_x formation. A comparison of capacitance density vs voltage for 1.4×10^{-4} and 5.2×10^{-4} cm^2 (~50 and ~125 μm diameter, respectively) area devices with $d_{Ti} = 10$ nm is shown in Fig. 5(b). Minimal areal dependence was seen for $d_{Ti} \leq 2.5$ nm. The reduced capacitance density for the smaller $d_{Ti} = 10$ nm device points to ambient oxidation around the perimeter. To determine the lateral extent of Ti oxidation, devices were modeled as an Al_2O_3 capacitor of the total area, A, in series with the combination of two parallel TiO_x capacitors: (i) an inner circular capacitor, C_{circ}, of area A_{circ}, with a thin TiO_x of thickness d_{TiO_x} formed by scavenging of O from Al_2O_3, and (ii) a surrounding outer ring shape capacitor, C_{ring}, with TiO_x of thickness $2d_{Ti}$ (to account for volume expansion) and area, A_{ring}, formed by complete oxidation of the Ti layer around the perimeter [illustrated in the inset in Fig. 5(b)]. The total capacitance of the device was modeled as

$$C_{tot} = C_{Al_2O_3} || (C_{circ} + C_{ring}) = C_{Al_2O_3}(C_{circ} + C_{ring})/(C_{Al_2O_3} + C_{circ} + C_{ring}), \quad (1)$$

where $C_{Al_2O_3} = \frac{\epsilon_{Al_2O_3} A}{d_{Al_2O_3}}$, $C_{circ} = \frac{\epsilon_{TiO_2} A_{circ}}{2d_{Ti}}$, and $C_{ring} = \frac{\epsilon_{TiO_x} A_{ring}}{d_{TiO_x}}$.

The relative dielectric constant of Al_2O_3, $\epsilon_{Al_2O_3}$, was determined to be 8.7 for the $d_{Ti} = 0$ nm device and ϵ_{TiO_x} was calculated to be 11 (assuming complete oxidation of Ti in $d_{Ti} = 0.5$ and 1 nm device). Solving the equations for the $d_{Ti} = 10$ nm device, resulted in a d_{TiO_x} of ~2 nm in the central circular region and a 4–6 nm extent of lateral Ti oxidation around the perimeter of the device (the ring). A d_{TiO_x} of ~2 nm in the central region suggests consumption of <2 nm of the Ti metal. This is consistent with the minimal area dependence seen for capacitance measurements of the devices with $d_{Ti} < 2.5$ nm (not shown), the lack of obvious TiO_x presence in the TEM [Fig. 1(b)], and the relative independence of the tailing and hump features on Ti thicknesses greater than 1 nm.

Given the capacitive evidence for a thin TiO_x layer, it is likely that in addition to a likely role for VO, the TiO_x layer also plays a role in the yield tailing and hump. One possibility is emission from the conduction band of the TiO_x interfacial layer. Electrons would be first excited from the Pt/Ti into the TiO_x conduction band and then into the Al_2O_3 conduction band or even into V_O levels. The barrier between Ti and TiO_2 is <1 eV, and the electron affinity difference between TiO_2 and Al_2O_3 is about 2.8 eV.[27,43] As the incoming photon energy increases, this multi-step path would be overwhelmed by direct emission from the metal, leading to the hump/increase in the yield slope at ~3.8 eV.

IV. SUMMARY/CONCLUSION

The impact of the interfacial Ti wetting layer thickness in as-deposited bilayer Pt/Ti electrodes was assessed using *in situ* IPE spectroscopy measurements of φ_{Bn}, the potential barrier between the electrode Fermi level and the Al_2O_3 conduction band edge. We found that a very thin 0.5–1.0 nm layer of Ti was sufficient to dominate φ_{Bn} and completely transition the effective work function from that of the Pt capping metal to that of the Ti wetting layer. Without Ti, $\varphi_{Bn,Pt/Al_2O_3}$ was found to be ~3.5–3.6 eV. The insertion of a 0.5–1 nm layer of Ti decreased $\varphi_{Bn,Pt/Ti/Al_2O_3}$ by ~0.5 to ~3.0 eV. Increasing the thickness of the Ti layer beyond 1 nm had little further influence, consistent with the reported dependence of the electrically extracted effective work function, $\Phi_{M,eff}$, for a variety of cap-metal/interface-metal/insulator systems.[16–19] It was also revealed that the Ti wetting layer pulled oxygen from AlO_3 and caused tailing (stretch out to lower energy) of the IPE yield curves, a potential drawback of using a highly reactive metal at the interface. For the electrode barrier opposite the Ti wetting layer, the measured $\varphi_{bn,Al_2O_3/TiN}$ were unchanged within experimental error, confirming that the changes in the top interface had little impact on the bottom barrier. This work shows that the composition of the metal immediately at the interface dominates not only the electrically extracted $\Phi_{M,eff}$, as shown by previous electrical measurements, but also φ_{bn}. The sharp transition of φ_{bn} with d_{Ti} is likely allowed by the limited diffusion of Pt to the interface in these unannealed devices.

Large work functions are often desired for low leakage MOS and MIM based devices as well as for qubits.[15] Although adhesion layers are necessary to form robust contacts between noble metals and oxides, we find that, in the absence of cap-metal diffusion, the addition of even a very thin wetting layer removes any *direct* influence of the cap-metal on φ_{bn}. For a very thin interfacial metal, the cap-metal might still *indirectly* influence the local φ_{bn}, potentially through strain mismatch and grain size. Concerning qubit operation, the use of an interfacial metal, thus, may allow decoupling of the influence of the cap metal/substrate strain mismatch, cap metal grain size and orientation, and cap metal work function from defects at the semiconductor interface.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jessica Haglund: Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **John F. Conley Jr.:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Project administration (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that supports the findings of this study are available from the corresponding author upon reasonable request.

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